

Fig.1

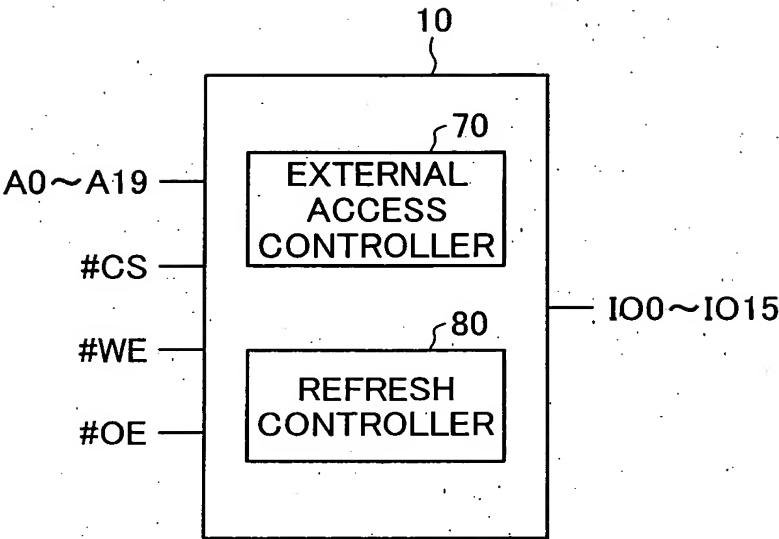


Fig.2

	#CS	REFRESH MODE (*)
OPERATION	L	MODE 1
STAND-BY	H	MODE 2

(*)

Refresh Mode 1: The refreshing operation starts synchronously with the output enable signal or the write enable signal after the generation of the refresh timing signal in the memory chip.

Refresh Mode 2: The refreshing operation starts according to the generation of the refresh timing signal in the memory chip (address input is not required).

Fig.3

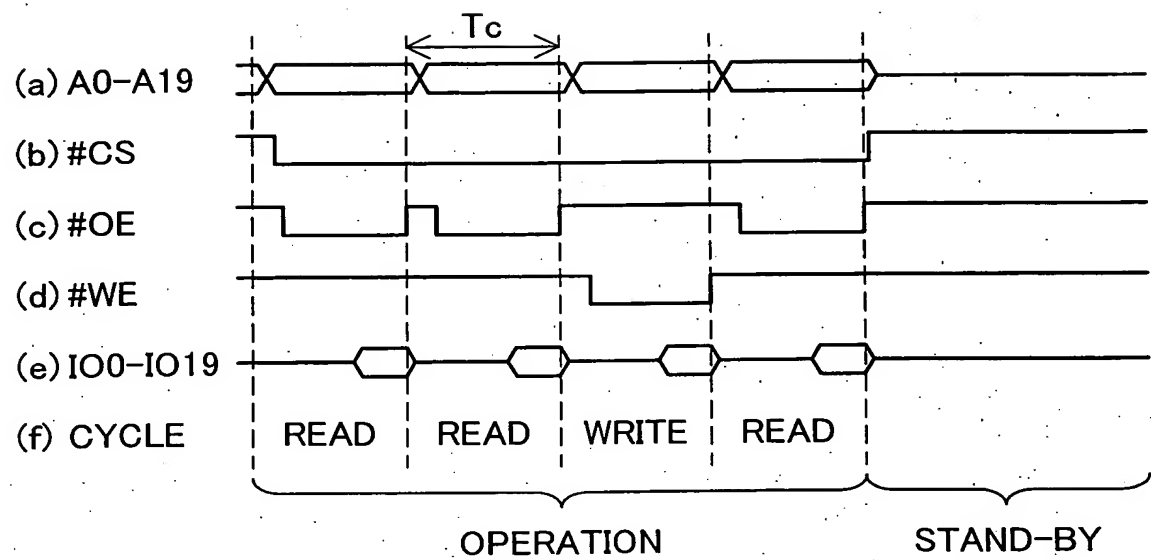
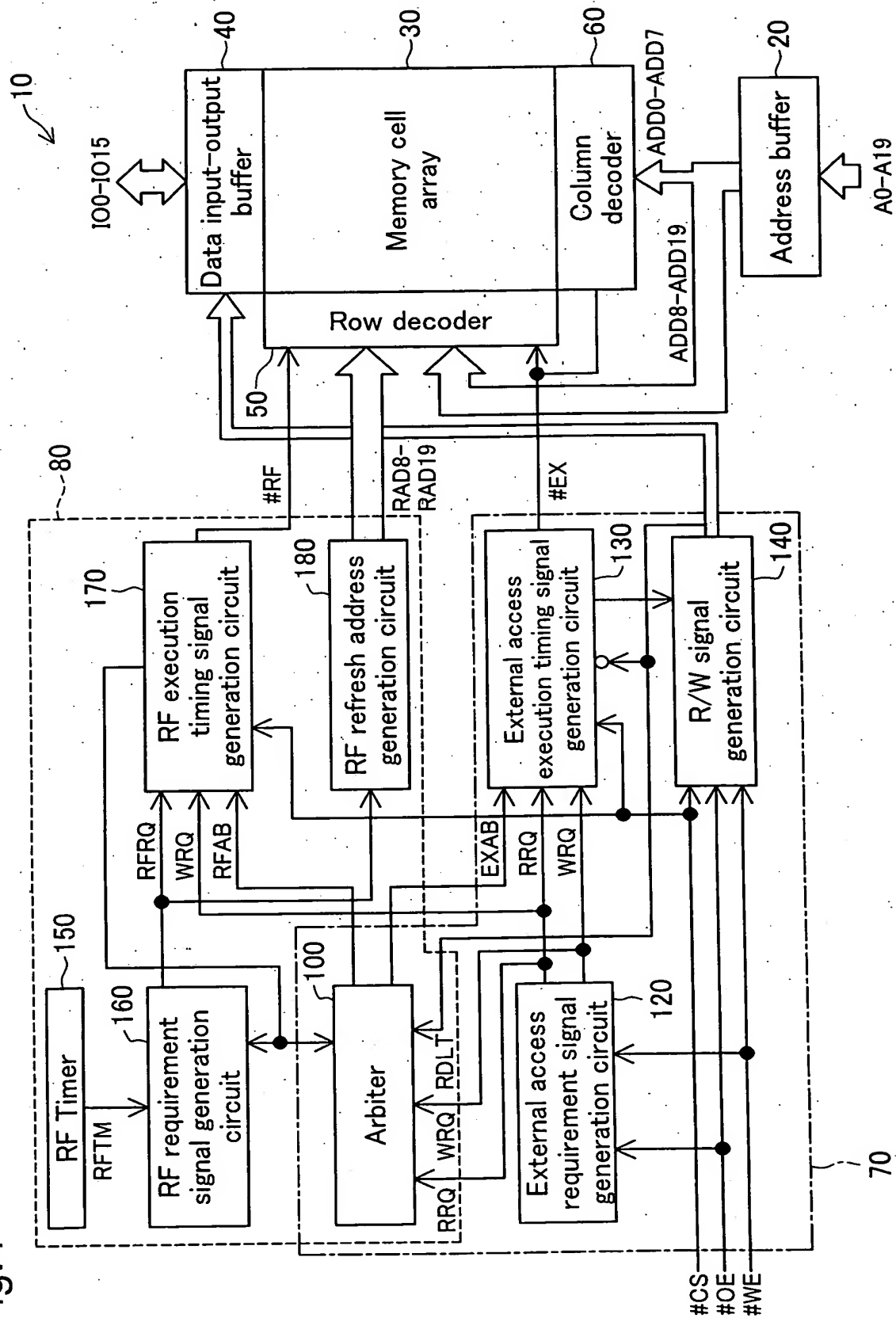


Fig.4



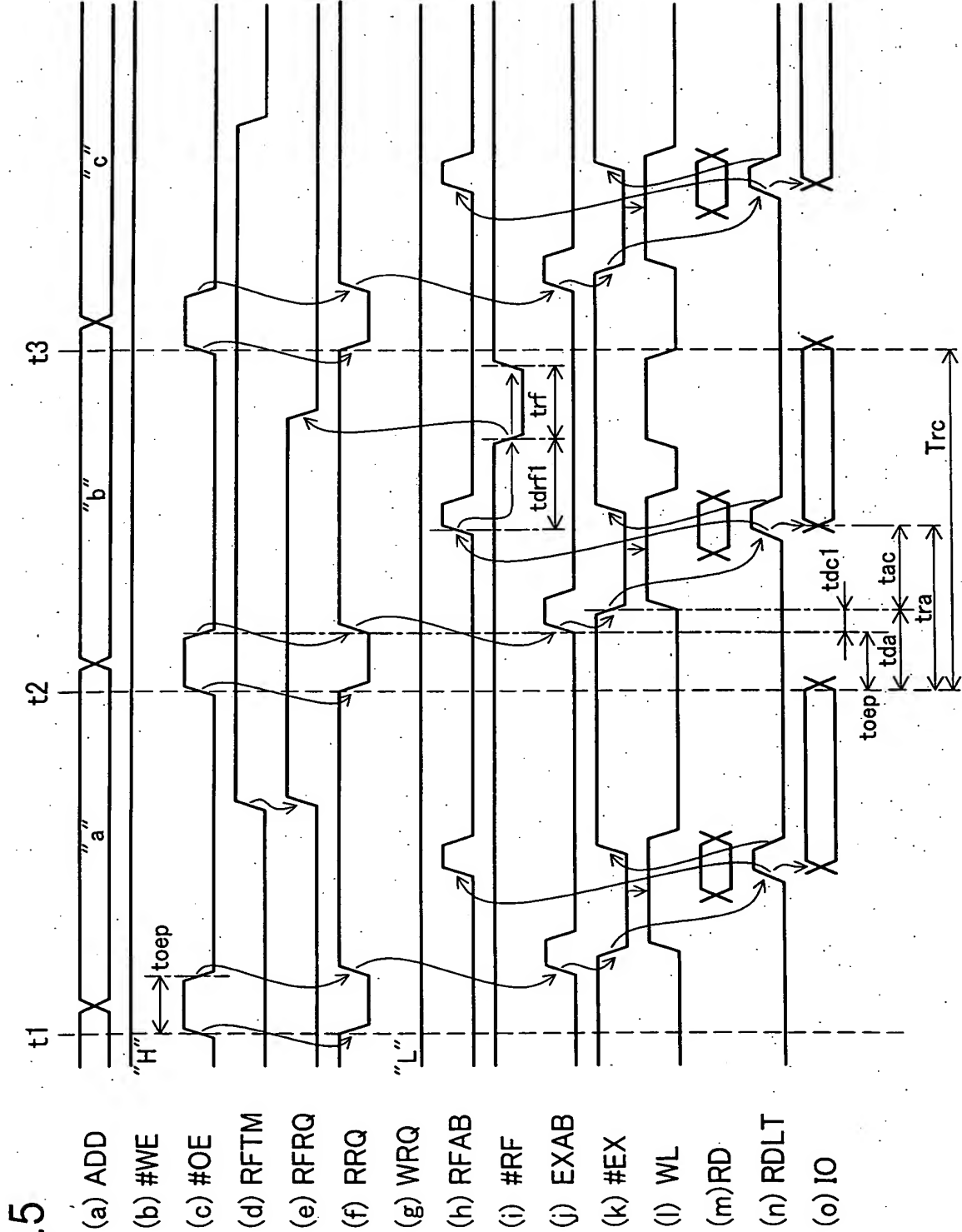
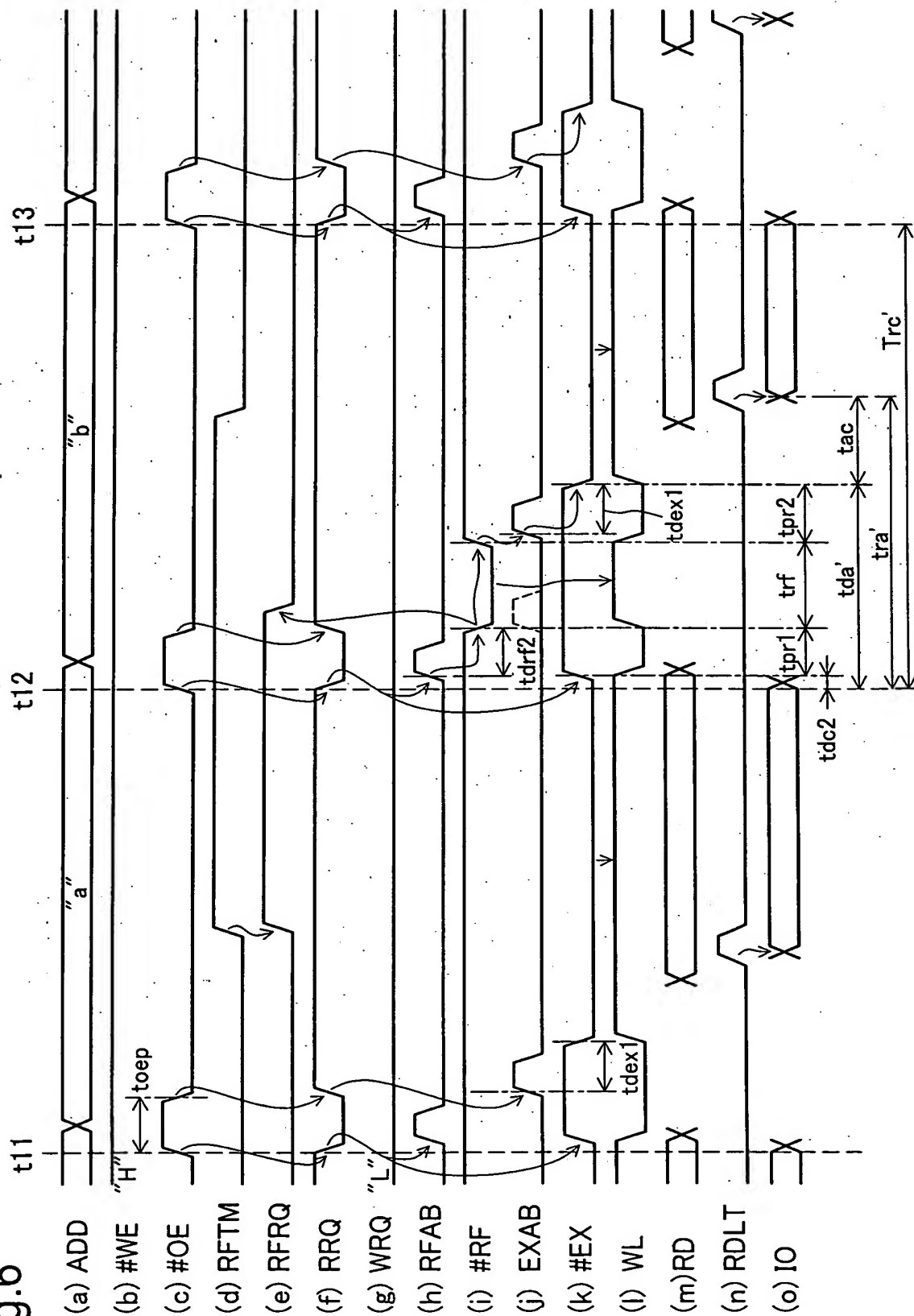


Fig.6



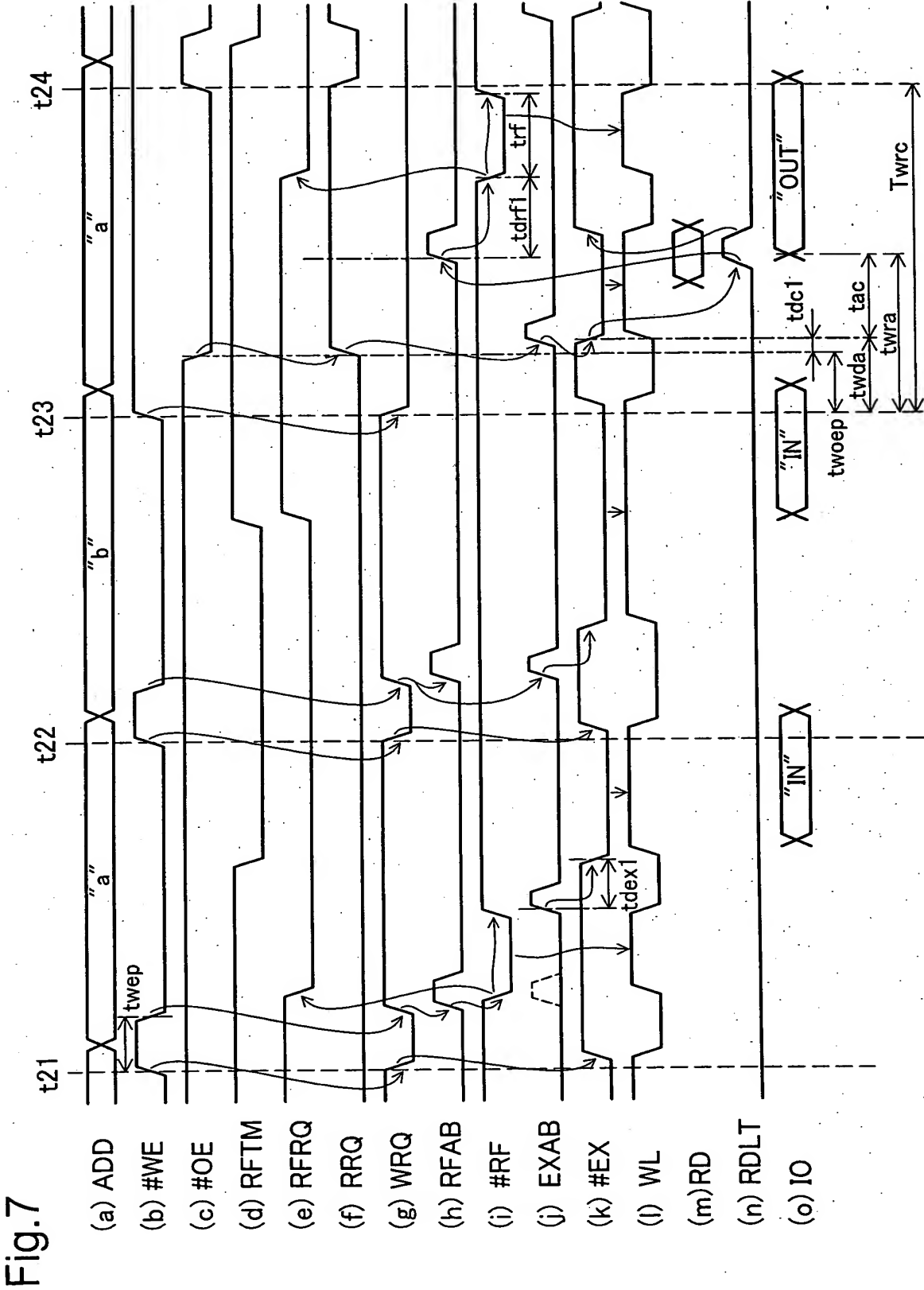


Fig. 8

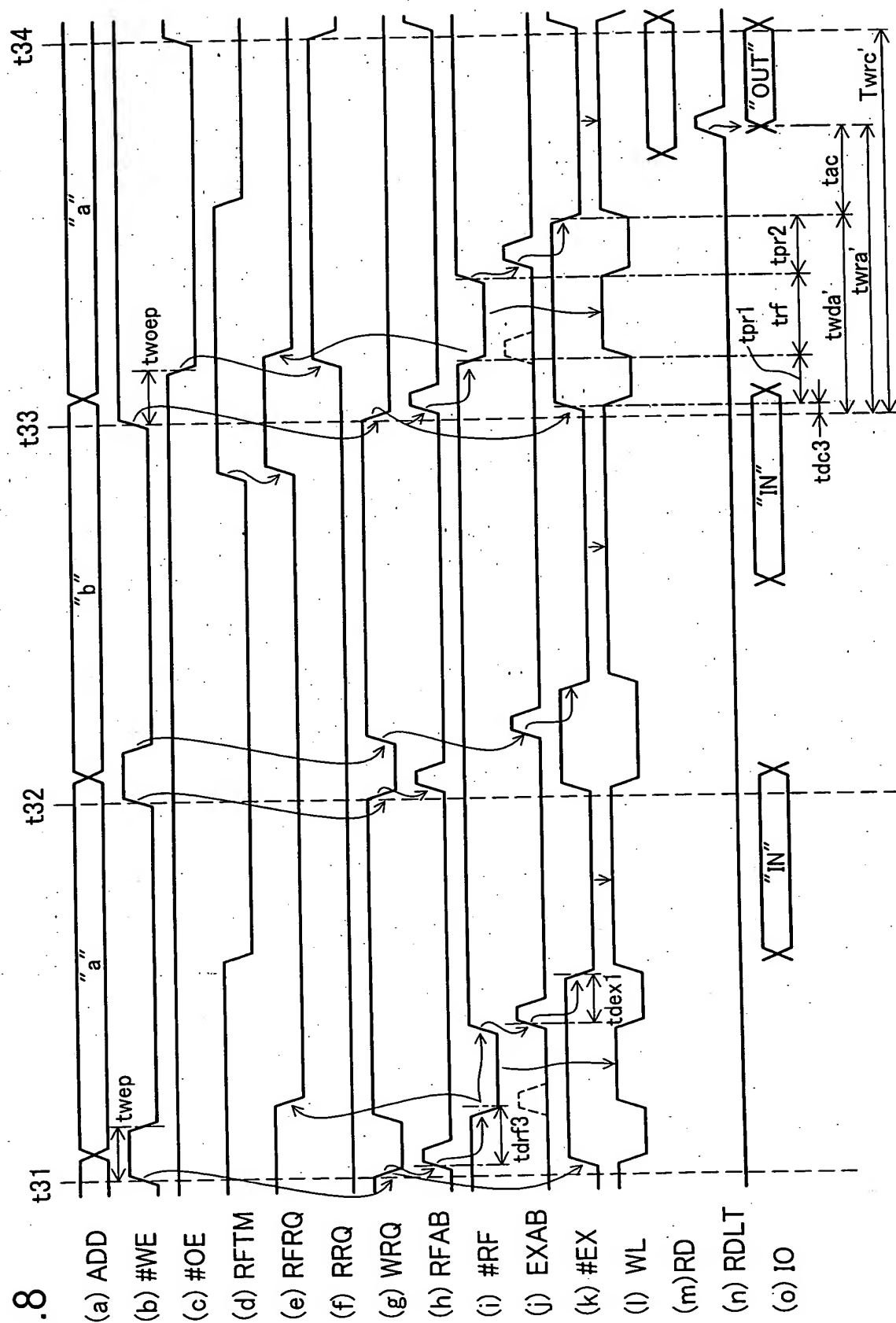


Fig.9

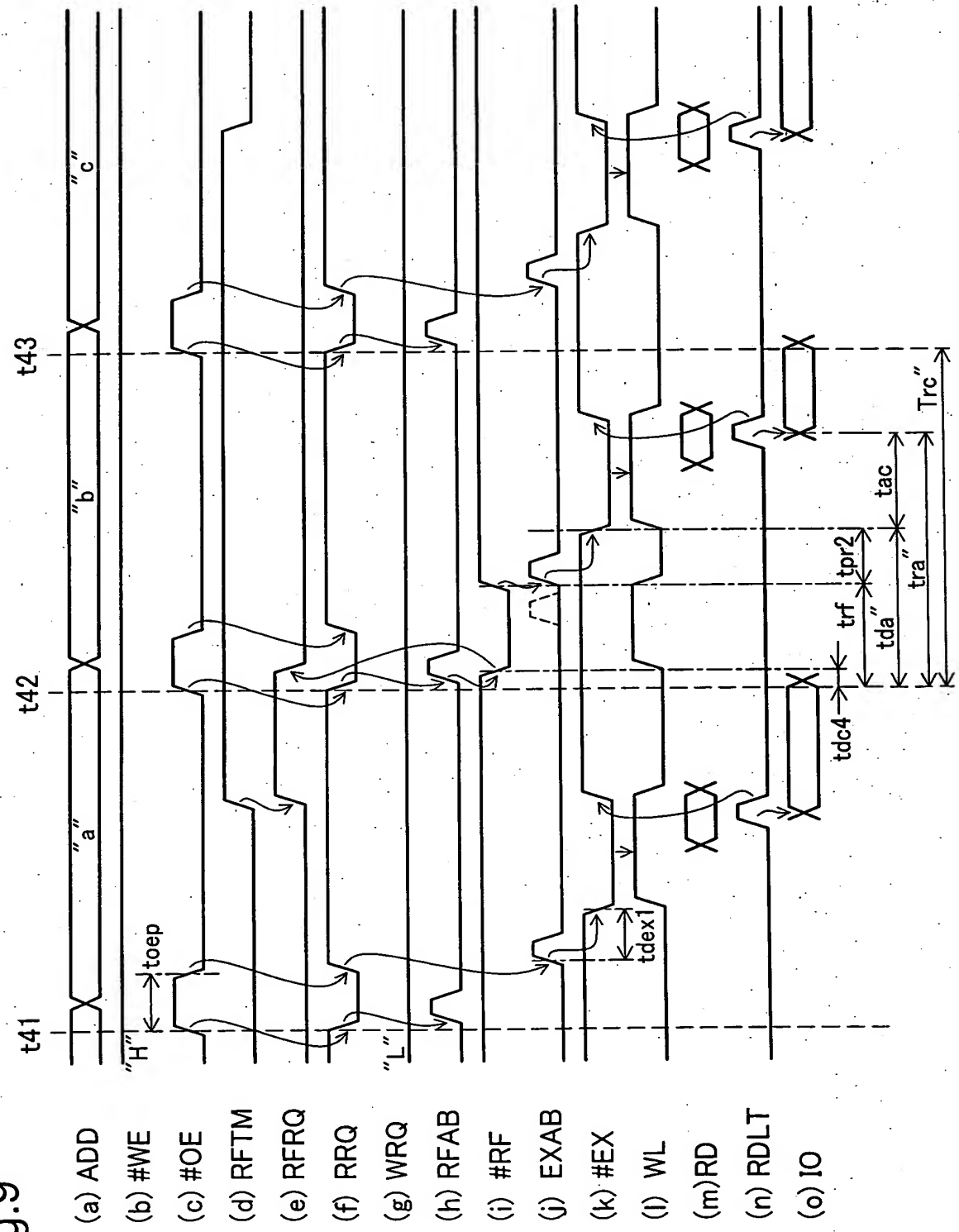


Fig.10

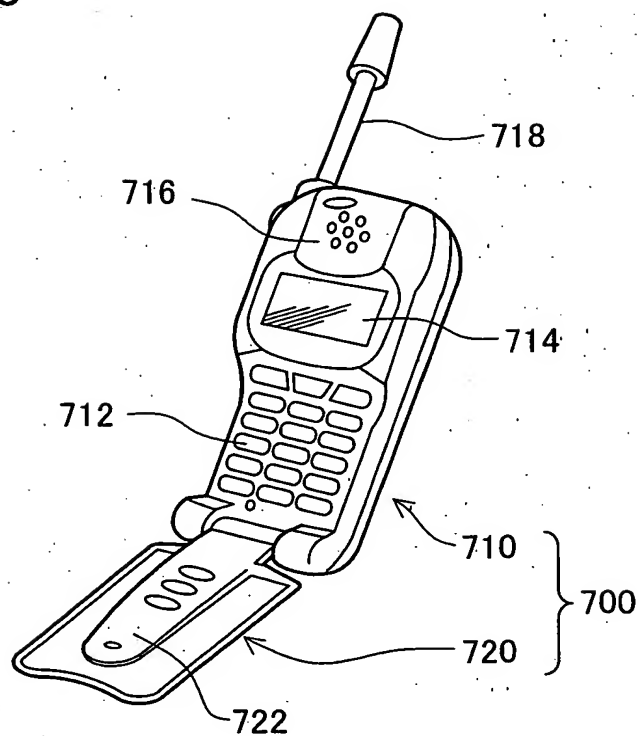


Fig.11

